



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant: Chia-Chung Wang et al.
Assignee: Bridge Semiconductor Corporation
Title: METHOD OF MAKING A SEMICONDUCTOR CHIP
ASSEMBLY WITH A CONDUCTIVE TRACE AND A
SUBSTRATE
Serial No.: 10/646,415 Filed: August 22, 2003
Examiner: Unknown Group Art Unit: Unknown
Atty. Docket No.: BDG018

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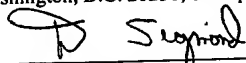
INFORMATION DISCLOSURE STATEMENT

Pursuant to Applicant's duty of disclosure under 37 C.F.R. § 1.56 and §§ 1.97-1.98,
Applicant hereby provides a copy of the documents identified on the enclosed Form PTO-1449.

The filing of this Information Disclosure Statement shall not be construed as a
representation that a search has been made, an admission that any of these documents, alone or in
any combination, is considered to be material to patentability, an admission that any of these
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This Information Disclosure Statement is filed before the mailing date of a first Office
Action on the merits. Accordingly, no fee is due. 37 C.F.R. § 1.97(b)(3).

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on September 2, 2003

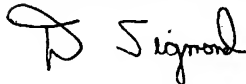


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9/2/03

Date of Signature

Respectfully submitted,



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Form PTO-1449				Atty Docket No.		Serial No.	
U.S. Department of Commerce, Patent and Trademark Office				BDG018		10/646,415	
 INFORMATION DISCLOSURE STATEMENT (Use several sheets if necessary)				Applicant			
				Chia-Chung Wang et al.			
				Filing Date		Group Art Unit	
				August 22, 2003			
U.S. Patent Documents							
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
	AA	5,149,958	09/1992	Hallenbeck et al.	250	216	
	AB	5,523,608	06/1996	Kitaoka et al.	257	433	
	AC	5,834,835	11/1998	Maekawa	257	680	
	AD	5,893,723	04/1999	Yamanaka	438	65	
	AE	5,929,516	07/1999	Heerman et al.	257	701	
	AF	6,001,671	12/1999	Fjelstad	438	112	
	AG						
	AH						
	AI						
	AJ						
	AK						
Other Art (Including Author, Title, Date, Pertinent Pages, Etc.)							
	AN	Harper, "Electronic Packaging and Interconnection Handbook," Third Edition, Published by McGraw-Hill, 2000, page 7.42.					
	AM	Towle et al., "Bumpless Build-Up Layer Packaging," 7 pages, downloaded from www.Intel.com on November 1, 2002.					
	AN	Towle et al., "Bumpless Build-Up Layer Packaging," 19 pages, dated November 11, 2001, downloaded from www.Intel.com on November 1, 2002.					
	AO	Teixeira, "Bumpless Build-Up Layer Packaging Technology," Intel Backgrounder, 4 pages, downloaded from www.Intel.com on November 1, 2002.					
	AP	Braunisch et al., "Electrical Performance of Bumpless Build-Up Layer Packaging," 15 pages, downloaded from www.Intel.com on November 1, 2002.					
	AQ	Braunisch et al., "Electrical Performance of Bumpless Build-Up Layer Packaging," 2002 Electronic Components and Technology Conference, 6 pages, downloaded from www.Intel.com on November 1, 2002.					
Examiner			Date Considered				
*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with your next communication to Applicant.							